

Customer No.: 31561  
Application No.: 10/707,016  
Docket No.: 12423-US-PA-X

**AMENDMENT**

Please amend the application as indicated hereafter.

**In the Claims :**

1-22. (canceled)

23. (original) A method for fabricating a memory device disposed in a substrate, the memory device comprising a plurality of pairs of word lines, a plurality of pairs of source lines and a plurality of source/drain regions, wherein the method for fabricating the memory device is characterized in that:

forming one pair of source lines that are electrically connected to each other between each pair of word lines, so that the source/drain regions are disposed beside each word line and each source line;

forming a dielectric layer over the substrate; and

forming a plurality of source line contacts, one source line contact being in the dielectric layer between each pair of the source lines, wherein each source/drain region between each pair of the source lines is electrically connected to at least one of each pair of the source lines by each source line contact.

24. (original) The method of claim 23, wherein the method is further characterized in that:

the word lines and the source lines are formed by patterning a same conductive layer.

25. (original) The method of claim 23, further comprising forming a plurality of

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bit line contacts in the dielectric layer, wherein the method is further characterized in that:

forming a plurality of source line contact openings and a plurality of bit line contact openings in the dielectric layer in a same process of photolithography and etching;  
and

filling a conductive layer into the plurality of source line contact openings and the plurality of bit line contact openings to form the plurality of source line contacts and the plurality of bit line contacts.

26. (original) The method of claim 23, further comprising forming a plurality of bit line contacts in the dielectric layer, wherein the method is further characterized in that:

forming a plurality of source line contact openings in the dielectric layer in a first process of photolithography and etching

forming a plurality of bit line contact openings in the dielectric layer in a second process of photolithography and etching; and

filling a conductive layer into the plurality of source line contact openings and the plurality of bit line contact openings to form the plurality of source line contacts and the plurality of bit line contacts.

27. (original) The method of claim 23, wherein the plurality of source line contacts is formed by forming a plurality of source line contact openings in the dielectric layer and then filling a conductive material into the plurality of source line contact openings, the method is further characterized in that:

each source line contact opening is a self-aligned contact opening, and the method further comprising:

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forming a conformal etching stop layer over the substrate, after forming the dielectric layer and before forming the plurality of self-aligned source line contact openings, and the step of forming the plurality of source line contact openings in the dielectric layer further comprising:

removing the dielectric layer covering the source/drain regions between each pair of source lines using the conformal etching stop layer as a stop layer, and at least removing the dielectric layer covering at least one of each pair of source lines, to form the plurality of the self-aligned source line contact openings; and

etching back the conformal etching stop layer exposed by the source line contact openings to expose the source/drain regions and at least expose one of each pair of source lines.

28. (original) The method of claim 23, further comprising forming a plurality of spacers on sidewalls of the word lines and the source lines, after forming the word lines and the source lines and before forming the dielectric layer, the method is further characterized in that:

forming a liner layer on the sidewalls of the word lines and the source lines before forming the spacers, and further comprising removing the spacers between each pair of the source lines to expose the liner layer after the step of forming the spacers.

29. (original) The method of claim 23, wherein the method is further characterized in that:

forming a plurality of isolation structures in strip shapes in the substrate, thus defining a plurality of active regions in strip shapes in the substrate, wherein the active

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regions are not connected to one another, and wherein the word lines are disposed in a direction vertical to the strip isolation structures and the strip active regions.

30. (original) A method for fabricating a memory device, comprising:

forming a plurality of strip isolation structures in a substrate to define a plurality of strip active regions in the substrate, wherein the plurality of the strip active regions includes a plurality of pairs of first channel regions in arrays and a plurality of pairs of second channel regions in arrays, and wherein each pair of the second channel regions are disposed between each pair of the first channel regions;

forming a first dielectric layer on the substrate;

forming a plurality of first gates and a plurality of second gates simultaneously, each first gate being disposed on the first dielectric layer above each first channel region and each second gate being disposed on the first dielectric layer above each second channel region;

forming a plurality of second dielectric layers, one of the second dielectric layers disposed on each first gate and on each second gate;

forming a first conductive layer over the substrate;

defining the first conductive layer to form a plurality of pairs of word lines and a plurality of pairs of source lines, wherein the word lines and the source lines are disposed in a direction vertical to the strip isolation structures and the strip active regions, while each pair of source lines are disposed between each pair of the word lines, and wherein each word line covers the second dielectric layers on the first channel regions of the same row and each source line covers the second dielectric layers on the second channel regions

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of the same row;

forming a plurality of source/drain regions in the substrate beside the word lines and the source lines;

forming a spacer on each sidewall of each word line and on each sidewall of each source line;

forming a third dielectric layer over the substrate;

forming a plurality of source line contact openings in the third dielectric layer, exposing the source/drain regions that are between each pair of source lines and at least exposing one of each pair of the source lines; and

filling a conductive material into the source line contact openings to form a plurality of source line contacts for connecting the source/drain regions that are between each pair of source lines and at least connecting one of each pair of the source lines.

31. (original) The method of claim 30, further comprising forming a conformal etching stop layer over the substrate before the step of forming the third dielectric layer and after the step of forming the spacer, wherein each source line contact opening is a self-aligned contact opening, and wherein the step of forming the source line contact openings further comprises:

removing the third dielectric layer covering the source/drain regions between each pair of source lines using the conformal etching stop layer as a stop layer, and at least removing the third dielectric layer covering at least one of each pair of source lines, to form the plurality of the self-aligned source line contact openings; and

etching back the conformal etching stop layer exposed by the source line contact

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openings to expose the source/drain regions and at least expose one of each pair of source lines.

32. (original) The method of claim 30, further comprising forming a liner layer on the sidewalls of the word lines and the source lines, after the step of forming the word lines and the source lines and before the step of forming the spacers, and further comprising removing the spacers between each pair of the source lines to expose the liner layer after the step of forming the spacers.

33. (original) The method of claim 30, further comprising forming a conformal etching stop layer over the substrate after the step of removing the spacers and before the step of forming the source line contact openings in the third dielectric layer, wherein each source line contact opening is a self-aligned contact opening, and wherein the step of forming the source line contact openings further comprises:

removing the third dielectric layer covering the source/drain regions between each pair of source lines using the conformal etching stop layer as a stop layer, and at least removing the third dielectric layer covering at least one of each pair of source lines, to form the plurality of the source line contact openings; and

etching back the conformal etching stop layer exposed by the source line contact openings to expose the source/drain regions and at least expose one of each pair of source lines.

34. (original) The method of claim 30, wherein each source line contact exposes one source/drain region in one strip active region between each pair of the source lines and exposes at least one of each pair of the source lines.

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35. (original) The method of claim 30, wherein each source line contact exposes at least two source/drain regions in at least two adjacent active regions between each pair of the source lines and exposes at least one of each pair of the source lines.

36. (original) The method of claim 30, further comprising:

forming a plurality of bit line contact openings in the third dielectric layer, so that each bit line contact opening exposes one source/drain region beside each pair of the word lines; and

filling a conductive material into the bit line contact openings to form a plurality of bit line contacts, wherein each bit line contact connects to one source/drain region beside each pair of the word lines.

37. (original) The method of claim 36, wherein the plurality of source line contact openings and the bit line contact openings are formed at the same time.

38. (original) The method of claim 36, wherein the plurality of source line contact openings and the bit line contact openings are not formed at the same time.

39. (original) The method of claim 30, wherein the step of the plurality of first gates and the plurality of second gates comprises:

forming a second conductive layer over the substrate;

defining the second conductive layer to form a plurality of second strip conductive layers, each second strip conductive layer disposed on each strip active region;

defining the plurality of the second strip conductive layers at the same time as defining the first conductive layer strip, to form the plurality of the first gates and the plurality of second gates.